J-11

CONTROL CHIP SPECIFICATION

21-17679-00

Rev. 3.03 (June 22, 1982)

C O M P A N Y C O N F I D E N T I A L

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RESERVED ISSUES

The following issues are reserved for the implementation effort and have no impact on contractual status or delivery. When these issues are resolved, the chip specifications will be updated accordingly.

1. Data Chip - EU register file codes. Harris may assign extra register select codes to ensure that all codes actually select a register.

   Freeze point: Data chip logic design review
   Status: Closed December, 1980

2. Data Chip - MMU register file codes. Harris may reassign register select codes to minimize internal logic.

   Freeze point: End June, 1980
   Status: Closed December, 1980

3. Data Chip - Opcodes. Within guidelines to be provided by DEC by end April 1980, Harris may assign currently unassigned opcodes to minimize internal logic.

   Freeze point: End June, 1980
   Status: Closed December, 1980

4. Control Chip - AIO codes. DEC may reassign AIO codes to minimize external logic.

   Freeze point: End April, 1980
   Status: Closed - no change to specification

5. Data Chip - NOP status flags. This is a don't care. NOP must have an opcode of 177 and must not alter the EU register file.

   Freeze point: End June, 1980
   Status: Closed December, 1980

6. Control and Data Chips - AC characteristics. By mutual agreement, Harris and DEC can adjust all non-critical parameters to minimize internal and external logic, within the following limits:

Control Chip AC Constraints

tpd + tps (MPRDC-L valid delay + setup) $\leq$ 75 ns

tseld + tsels (MCSEL-L active delay + setup) $\leq$ 75 ns

tmibs + tmibd (MIB-H valid delay + setup) $\leq$ 75 ns

Interchip AC Constraints

tscs + tsid (MSCTL-L setup + inactive delay) $\leq$ 50 ns

tmibs + tmibd (Data Chip + Control Chip) $\leq$ 75 ns

tpd + tprds (MPRDC-L valid delay + setup) $\leq$ 75 ns

MKPB-L, MSOV/JA-L must be valid by T100 and held to T150

Freeze point: End of pass 3 of Control Chip
Status: Open

7. Data Chip - I/O multiplexor. Within the functional and timing constraints of the Data Chip Specification, Harris can implement the I/O multiplexor as it chooses to minimize layout area and/or logic.

   Freeze point: Data Chip logic design review
   Status: Closed December, 1980

8. Data Chip - UMULS, SMULS, DIVS microinstructions. These microinstructions are shown as implemented for all operand lengths. Should a subset implementation save logic in the Data Chip, only the following lengths need be implemented:

   UMULS - longword
   SMULS - word
   DIVS - word, longword

   In particular, support of byte length operands need not be implemented.

   Freeze point: Data chip logic design review
   Status: Closed - byte length not implemented

9. Data Chip - Crystal input parameters. The crystal input AC parameters and test conditions will be specified when DEC selects an input crystal for the Chip set.

   Freeze point: End April, 1980
   Status: Open, extended until December, 1982

10. Control and Data Chips - DC characteristics. The TTL input parameters (V_{IHT} and V_{ILT}) are goals and are subject to change as simulation results become available. Harris and DEC can adjust these parameter by mutual agreement.

    Freeze point: End April, 1980
    Status: Open, extended until December, 1982

11. Data Chip - Clock outputs. Input test conditions are tbs.

    Freeze point: End June, 1980
    Status: Open, extended until December, 1982

12. Data Chip - MDAL-H turnaround. The test specification is for an isolated chip. In a real system, the Data Chip will be fighting with another driver. By mutual agreement, Harris and DEC can adjust the test specification on MDAL-H turnaround to more accurately reflect actual operating conditions.

    Freeze point: End April 1980
    Status: Closed - no change to test specification

REVISION HISTORY

REV	DATE	REASON
3.03	6/24/82	Incorporated specification changes 1c, 106-110, 113, 115-117, 119-120, 122-123, 126-130 of Rev 13 of the Specification Change list dated June 22, 1982.
3.02	2/9/81	Incorporated specification changes 1b, 30, 34, 36-57, 59-62, 64-81, and 83-104 of Rev 9 of the Specification Change list dated February 9, 1981.
3.01	7/14/80	Incorporated specification changes 1, 3, 5, 7, 13, 15, 19, 24, 25, 26, 27, and 28 of Rev 4 of the Specification Change list dated June 16, 1980.
3.00	4/16/80	Incorporated specification number.
2.00	1/80	Added abort service logic, parity error logic, signal polarities. Revised DC characteristics. Cleanup of Rev 1.02.
1.02	8/27/79	Specified Q logic and service logic.
1.01	6/29/79	Increased array size and detailed more logic.
1.00	5/14/79	Preliminary.

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1.0 INTRODUCTION

1.1 Scope

This document specifies the design of a MOS/LSI chip which is part of a chip set that implements a high performance PDP-11 processor with Memory Management, FP-11 Floating Point, and CIS Commercial Instructions. This specification describes the internal organization and characteristics of the Control chip. This specification does not describe the operation of the PDP-11 or other chips in the chip set. For further information, the applicable documents should be consulted.

1.2 Applicable Documents

J-11 Programmer's Reference
PDP-11/70 Processor Handbook
J-11 Chip System Specification
J-11 Data Chip Specification
J-11 Microprogrammer's Reference

1.3 Control Chip Organization

The Control chip contains the microprogram sequence logic as well as 1280 words of local microprogram storage in Programmed Logic Array (PLA) and Read Only Memory (ROM) arrays. Architecturally, there are several major function blocks in the chip: the microstore array, the next address logic, the counter logic, the prefetch logic, the interrupt service logic, the abort service logic, the AIO code generator, the coprocessor support logic, and the state sequencer. These blocks are connected by several major internal busses including the 22-bit Microinstruction bus (IMI<21:0>), which drives the 22-bit external Microinstruction Bus (MIB-H<21:0>) and the 17-bit internal Microinstruction bus (IMIB<21:5>); the 10-bit Next Address Field bus (NAF<9:0>); the 10-bit Next Address bus (NA<9:0>); and the 16-bit internal Data and Address bus (IDAL<15:0>), which reads off the external Data and Address Bus (MDAL-H<15:0>). During the course of a microcycle, the chip accesses the appropriate microinstruction from the microstore, sends it along the external Microinstruction Bus (MIB) to the Data chip for execution, and simultaneously generates the address for the next microinstruction to be accessed. Note that the Control chip is responsible for accessing only its local storage. Architecturally, multiple Control chips (up to 32) can be used to provide additional microstore. Electrically, the number of Control chips is limited by the capacitance budget of the MIB at specified speed.

1.4 Internal Busses

The Control chip is organized around the following internal busses:

- The Internal Data and Address bus (IDAL<15:0>) is an internal extension of the external Data and Address Lines (MDAL-H<15:0>). IDAL<15:0> can be driven by the IDAL latch, which captures information off the external MDAL bus, by the interrupt service logic, by the abort service logic, and by the coprocessor support logic. IDAL<15:0> is an input to the PLA input registers (PIR[1:0]), the Q logic input registers (QIR[1:0]), the counter logic, and the microsubroutine stack.

- The Next Address Field bus (NAF<9:0>) carries the next address output of the microstore array. NAF<9:0> is driven by the microstore array in normal mode or by the Next Address bus (NA<9:0>) in selected test modes. It is an input to the ID/RFS detection logic and, through the NAF latch, to the Next Address bus.

- The Next Address bus (NA<9:0>) carries the next address input to the microstore. NA<9:0> can be driven by NAF<9:0>, the microsubroutine stack, the conditional jump address register (CJAR<9:0>), or the Internal Microinstruction bus (IMIB<14:5>). One or more bits may be discharged (zeroed) by the Q logic, counter logic, or abort logic. NA<9:0> is an input to the microstore ROM and PLA decoders.

- The Next Address Test bus (NAT<9:0>) carries the data on the Next Address bus (NA<9:0>) to the Microinstruction bus (IMI<21:12>). It is used only in testing to make the data on the Next Address bus visible on the external Microinstruction bus (MIB-H<14:5>).

- The Microinstruction bus (IMI<21:0>) carries the microinstruction output of the microstore array. IMI<21:0> can be driven by the microstore array, the Next Address Test bus (NAT<9:0>), or the external Microinstruction bus (MIB-H<21:0>). One or more bits may be discharged or precharged by the initialization logic, the abort logic, and the chip select logic. IMI<21:12> is an input to the AIO code logic, to the external MIB drivers; and, through the IMIB latch, to the Internal Microinstruction bus (IMIB<21:5>).

- The Internal Microinstruction bus (IMIB<21:5>) carries the high order 17 bits of the current microinstruction. IMIB<21:5> is only driven by IMI<21:5> through the IMIB latch. It is an input to the jump logic, the state sequencer, the microsubroutine stack, and the Next Address bus (NA<9:0>).

1.5 Major States

At its maximum operating frequency (20 Mhz), the Control chip can potentially enter a new state every 25 nsec. The major states in a microcycle are as follows:

State	Time	Action
T0	(0 nsec)	Start of microcycle Initiate microstore access Drive MPRDC-L if predecode
T25	(25 nsec)	
T50	(50 nsec)	Physical address valid on MDAL-H, strobe IDAL latch if write Bank select valid on MBS-H<1:0>, clock BSFF<1:0> Clock interrupt synchronizer flip-flops Conditional jump decoding Clock ABFF<2:1> if demand bus cycle Strobe DATAV if prefetch
T75	(75 nsec)	Strobe PRDCFF
T100	(100 nsec)	Deassert MPRDC-L Toggle PIR/QIR output select of deselected chip if PRDCFF Update PIR/QIR input select latch if selected Clock ITFF flip-flop Clock service flip-flops Clock ABFF<4> if demand bus cycle
T125	(125 nsec)	Microstore access complete, drive IMI, NAF, MIB if selected Clock ISOVFF flip-flop Update PIR/QIR input select latch if deselected
T150	(150 nsec)	Read and status data valid on MDAL-H, strobe IDAL latch if read or output status Toggle PIR/QIR output select of selected chip if NAF=477
T175	(175 nsec)	

If the microcycle is not extended, the next state is TEND. If the microcycle is extended, operations proceed as follows:

State	Time	Action
T225	(225 nsec)	Write data valid on MDAL, strobe IDAL latch if write
Tx25	(225, 325 ... nsec)	
T250	(250 nsec)	Strobe PS or PIRQ with IDAL data if write
Tx50	(250, 350 ... nsec)	Clock interrupt synchronizer flip-flops Strobe DATAV if prefetch Sample MSCTL-L synchronizer flip-flop for continuation
Tx75	(275, 375... nsec)	
Tx00	(300, 400... nsec)	Clock interrupt flip-flops Clock ABFF<3> if demand bus cycle

All microcycles conclude as follows:

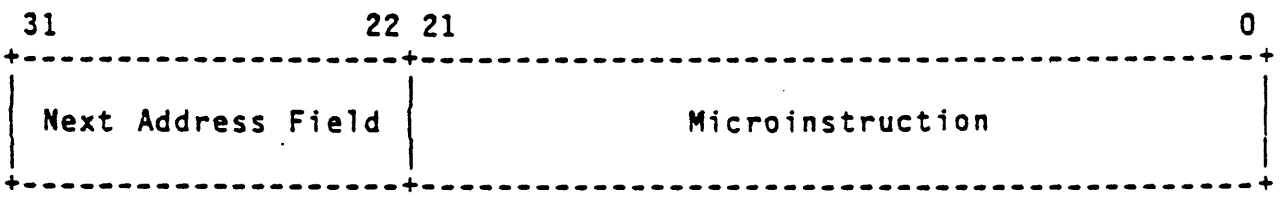
State	Time	Action
T-25	(175 if not stretched, else 375, 475... nsec)	Microinstruction valid on MIB, strobe IMIB latch Strobe QIR with IDAL data if prefetch Strobe PIR with IDAL data if prefetch or output status Strobe PS with IDAL data if output status Initiate Q logic if predecode Gate CJAR to NA if conditional jump Gate stack to NA if RFS Gate jump address to NA if deselected Gate NAF to NA otherwise Drive AIO codes if selected
TEND	(200 if not stretched, else 400, 500... nsec)	Clock ABFF<0> if demand bus cycle

2.0 FUNCTIONAL CHARACTERISTICS

This section describes the functional characteristics of the Control chip (refer to the block diagram at the end of the specification).

2.1 Microprogram Storage

The heart of this chip is the 1280 word microprogram storage. The microstore address space (0000-1777 octal) is divided into two sections, with the PLA responding to addresses 0400-0777 (octal) and the ROM responding to addresses 0000-0377 and 1000-1777 (octal). The PLA section consists of two banks of 256 minterms (total 512 terms) and the ROM section consists of three banks of 256 words (total 768 words). Each ROM word and PLA term stores a 32-bit word containing the 22-bit microinstruction and the 10-bit next address field needed for a microinstruction cycle. The format of the microstore word is shown below:



2.1.1 Programmable Logic Array (PLA)

The PLA section generates a 32-bit microstore word based on inputs from the Next Address bus (NA<6:0>) and external data and service information in the 17-bit PLA input registers (PIR<16> and PIR[1:0]<15:0>). The PLA may be programmed so that an address accesses a single location (like the ROM), or programmed so that an address acts as a translation code to access several locations. The PIR inputs may then be used in the latter case to further delimit the accessed location(s). Note that more than one PLA term can be active at a time, yielding a logically wire-ANDed output word.

The PLA section is subdivided into two banks of 256 terms. One bank responds to next address inputs 0400-0577 (octal), the other to inputs 0600-0777 (octal). (Thus no more than 256 PLA terms can be active in any one access.) Each PLA bank consists of an AND array and an OR array. During the microcycle, the PLA AND array decodes the PLA address (NA<6:0>) and the selected PIR (PIR<16> and PIR[1:0]<15:0>) inputs to select the desired PLA term(s). This information is then used by the PLA OR array to derive the appropriate 32-bit PLA output. Note that a reference to the PLA section that does not access a programmed PLA term results in a PLA output of all ones. This is interpreted as a next address of 1777 (octal) and a NOP microinstruction (see Data Chip Specification).

The OR word of a programmed PLA term can not have bits<21:0> equal to all 1's. This does not mean that the NAF can not be all 1's, or that a ROM word can not be all 1's, or that an unused (unprogrammed) PLA term can not be all 1's. Unprogrammed PLA term's OR array word must generate all ones.

2.1.2 Read Only Memory (ROM)

The ROM section consists of 768 words divided into 3 ROM banks, 256 words in the address space 0000-0377 (octal) and the remaining 512 in the address space 1000-1777 (octal). Each ROM word is 32 bits wide. Each ROM address accesses one and only one ROM word.

2.1.3 ROM/PLA Output Select

The outputs of the ROM and PLA sections of the microstore are selectively driven onto the microstore output busses (IMI<21:0> for the microinstruction, NAF<9:0> for the next address field) under the control of the three high order bits of the Next Address bus (NA<9:7>). If NA<9:8> = 01, then the PLA bank selected by NA<7> is enabled onto the busses; otherwise, one of the three ROM banks is enabled:

NA<9:7>=	Select	Decode From
00X	ROM bank 0	NA<7:0>
010	PLA bank 0	NA<6:0>'PIR<16:0>
011	PLA bank 1	NA<6:0>'PIR<16:0>
10X	ROM bank 1	NA<7:0>
11X	ROM bank 2	NA<7:0>

2.2 Next Address Logic

The next address used for the microinstruction fetch is generated at the end of the previous microcycle from a variety of sources: the next address field associated with the current microinstruction, the jump address field associated with an unconditional or conditional jump microinstruction, or the top of the microsubroutine stack. Only one of these four sources can drive the NA bus during any given microcycle. This address may then be altered by override logic which may discharge (zero) some of the next address bits.

2.2.1 Jump Logic

The Control chip recognizes two kinds of jumps: unconditional jumps, and conditional jumps. On an unconditional jump, the jump address field of the external microinstruction (IMIB<14:5>) is gated onto the Next Address bus. On a conditional jump, the jump address field of the previous microinstruction (CJAR<9:0>) is conditionally gated onto the Next Address bus. Consequently, unconditional jumps can be used to cross between chips; conditional jumps cannot cross between chips.

2.2.1.1 Unconditional Jump Logic

When the Control chip is deselected, it automatically gates the jump address field of the external microinstruction (IMIB<14:5>) onto the Next Address bus. If the Control chip then becomes selected, that is, if the microinstruction was a jump to this Control chip, then the jump address becomes the next address input to the microstore. If the Control chip remains deselected, then the microstore access is suppressed, and the jump address is effectively ignored. Note that a jump within the selected chip is effectively a NOP, that is, the next address is taken from the NAF.

2.2.1.2 Conditional Jump Address Register (CJAR<9:0>)

This 10-bit register is loaded from IMIB<14:5> every microcycle at T50 and is used with the Stack Overflow/Jump Allow (MSOV/JA-L) input and conditional jump decode logic to specify the next address on conditional jumps.

2.2.1.3 Conditional Jump Logic

This logic generates the control signals for the CJAR register. It consists of a flip-flop for recording whether the previous microinstruction was a conditional jump, and an enable on the output of the CJAR register. At T50, IMIB<21:15> is decoded. The flop is set to 1 if the microinstruction is a conditional jump, to 0 otherwise. At the following T-25, if the output of the flop is a 1, and the MSOV/JA-L signal is asserted (conditional jump taken), and the chip is selected, CJAR is gated onto the Next Address bus.

2.2.1.4 Chip Select Logic

The chip select logic determines whether this chip is the active Control chip. Each Control chip is mask-programmed with a unique chip identity code in the range 0 - 31 (decimal). A Control Chip is selected by executing a jump microinstruction with the chip select field equal to its mask-programmed identity code. At initialization or during a chip select error, all Control chips output a jump to chip 0 microinstruction onto the MIB; therefore, chip 0 will become selected at the next T0.

Prior to the beginning of each microcycle i.e., at T150 of the previous cycle, all Control chips precharge the MCSEL-L output high. Control chip 0 then sustains this high state with a small sustainer device. The selected Control chip pulls down MCSEL-L. All Control chips monitor this line and detect if MCSEL-L is not pulled low. If MCSEL-L is not pulled low, this implies that no Control chip was selected, and a chip select error occurs. Chip 0 will drive a jump to chip 0, ROM word 1 on the MIBS. This will cause a jump to ROM word 1 of Control chip 0. For time sequencing of MCSEL-L precharge, hold, and pull down, see the timing diagrams.

2.2.2 Microsubroutine Capability

The Control chip has a two-word deep microsubroutine stack which is pushed under microprogram control with the data from IMIB<14:5> or IDAL<9:0>. The most recent word already in the stack is pushed to the bottom of the stack, and the old bottom word is lost. When the stack is popped under microprogrammed control, the top of the stack is used as the next address (subject to next address overrides, Section 2.2.3), and then the contents of the top and bottom of the stack are exchanged. This is accomplished by the toggling of the micro-stack register select flip-flop. A Load Microstack (LMSTK) microinstruction is used to push the jump address field (IMIB<14:5>) onto the stack; an OUTS microinstruction with control bit<8> = 0 is used to push external data (IDAL<9:0>) onto the stack. A next address field of RFS = 0777 (octal) gates the top of the microsubroutine stack onto the Next Address bus and pops the stack. This condition is detected by the ID/RFS detect logic.

If a next address of RFS is present at the same time a conditional jump is taken (see Sect. 2.2.1.3), then the microstack will not be affected and the contents of the microstack will not be gated to the Next Address bus. Note: the microcode is restricted from setting NAF = RFS during a LMSTK microinstruction or an OUTS microinstruction with control bit<8> = 0.

2.2.3 Next Address Overrides

The next address, which is used to access the next microinstruction, can be dynamically altered by the override logic. This logic selectively discharges (zeroes) certain NA bits as a quick method to affect the next address. The abort, Q logic, and counter logic overrides only affect the Next Address bus.

2.2.3.1 Abort Override

If the MABORT-L input is asserted during a demand bus operation (see section 2.9.3), NA bits<9:8,6,4:0> are discharged (zeroed) at T-25/T25 of the next microcycle only. This override only occurs during demand bus operations (see section 2.9.3) and is ignored on request bus operations. This forces a next address of 0, 40, 200, or 240 (octal) where microcode routines reside to handle bus errors, memory management aborts, etc. For additional actions connected with MABORT-L, see section 2.6.

2.2.3.2 Counter Logic Override

If the current microinstruction will decrement the counter in the selected Control chip to zero, NA bit<0> is discharged (zeroed) at the beginning of that microcycle.

2.2.3.3 Q Logic Override

NA bits<5:0> may be discharged (zeroed) by the Q logic. This option, the enabling of which is mask programmable, can selectively discharge one or more of these bits based on the selected Q logic input register (QIR) contents, which will contain the macroinstruction when the next address has certain values. When the microprogram sequence reaches certain branch points in the operand fetch and instruction decode routines, the Q logic determines the next microaddress based on the instruction type and the operand addressing mode. The other inputs to the Q logic are the DATAV logic, the PPCV logic, ID1SVC, and the ID/RFS detection logic (see below). The Q logic overrides are detailed in Table 2-1.

2.2.3.3.1 PLA Prefetch Buffer Data Valid (DATAV)

This flip-flop indicates whether the data in the non-selected PLA input register (which is the effective PLA prefetch buffer, PPB) is valid or not. During prefetch microcycles, the MABORT-L input indicates whether the data on the MDAL is valid data or not.

DATAV is set on any prefetch (unless RDI and DATAV = 0) which does not result in an abort. This is accomplished by opening the DATAV latch at T50 and closing it at T-50 during all prefetch cycles. The DATAV latch input is derived from the following equation:

$$DATAV = -(MABORT\text{-}L + (RDI \cdot -DATAV))$$

DATAV is also cleared by assertion of the Kill Prefetch Buffer signal (MKPB-L). This flip-flop is an input to the Q logic and to the predecode signal (MPRDC-L) logic.

2.2.3.3.2 Physical PC Valid (PPCV)

This flip-flop indicates whether the Data chip physical program counter (PPC) is valid or not. This flip-flop is set by synchronization (RSYNC) and macro-branch (AOBC, SOBC) microinstructions. It is cleared by assertion of the Kill Prefetch Buffer signal (MKPB-L). If both MKPB-L and AOBC/SOBC occur, then PPCV should be set. This flip-flop is an input to the Q logic.

2.2.3.3.3 Interrupt Service (ID1SVC)

This input to the Q logic is defined by the following logic equation:

```
ID1SVC = (PTYFF + ITFF + ISOVFF + PWRFF + HLTFF + FPEFF +
          acknowledged interrupts).-SSFF
```

The inputs are, in order, the parity error flip-flop (see section 2.5.6), the intermediate T-bit flip-flop (see section 2.5.7), the stack overflow flip-flop (see section 2.5.8), the power fail, halt, and floating point exception flip-flops (see section 2.5.9), the output of the interrupt blocking logic (see section 2.5.5), and the single-step flip-flop (see section 2.8.2). Spurious interrupts will force IDISVC, however, the corresponding service flip-flop may <u>not</u> be set.

2.2.3.3.4 Q Logic Input Registers (QIR[1:0]<15:3>)

The Q logic receives instruction stream input from a pair of thirteen-bit Q logic input registers (QIR[1:0]<15:3>). At any instance, one of the two registers is selected for input to the Q logic, while the other is deselected and is waiting for or contains the next instruction stream word.

QIR selection rules:

1. In the selected Control chip, at T150 of a microcycle which generated a NAF of 477, toggle the output select flip-flop. In the deselected Control chip(s), at T100 of a MPRDC-L microcycle, toggle the output select flip-flop.
2. From T125 to T-25 of any prefetch (RDI, RDF, operate . control bit<12>=0 . DATAV=1), latch the input selected QIR from IDAL.
3. From T75 to T125 of all microcycles, update the input select latch with the opposite output select flip-flop information.

2.2.3.3.5 ID/RFS Detection Logic

This logic decodes the next address field (NAF<9:0>) to detect five special microaddresses: ID1 = ((NAF=0477 (octal)) AND (-Demand Abort)), ID2 = 0474 (octal), IDX = 0470-0477 (octal), IRDF = ((NAF=0460 (octal)) AND (-Demand Abort)), and RFS = 0777 (octal). The ID1, ID2, IDX, and IRDF outputs of this logic are inputs to the Q logic. The ID1 output is also an input to the predecode signal (MPRDC-L) logic. The RFS output is an input to the microsubroutine stack logic.

Table 2-1

Specification of Q Logic Overrides

Next microaddress in macroinstruction decode and execute routine (decoded from NAF<9:0>):

ID1 = 0477 (octal) AND -DEMAND ABORT ;entry point to macroinstruction decode

ID2 = 0474 (octal) ;exit point from source operand fetch

IDX = 0470-0477 (octal) ;all branch points in operand fetch

IRDF = 0460 (octal) AND -DEMAND ABORT ;entry point to refill prefetch pipeline

Special PDP-11 instruction classes (decoded from opcode in QIR):

SOPS = all single operand instructions (SWAB, CLR, COM, INC, DEC, NEG, ADC, SBC, TST, ROR, ROL, ASR, ASL, SXT, XOR, MFPI, MFPD, MFPS, MTPS, MUL, DIV, ASH, ASHC, and CSM)

DOPS = all double operand instructions (MOV, BIT, CMP, ADD, SUB, BIC, and BIS)

JOPS = all JUMP/JSR instructions (JMP and JSR)

Special PDP-11 addressing modes (decoded from mode in QIR):

SM0 = source mode 0

DM0 = destination mode 0

Special inputs to the Q logic:

ID1SVC = synchronous interrupt pending and not single-step (parity error interrupt, T-bit trap, stack overflow, power fail interrupt, halt line asserted, floating point exception, hardware interrupt requests or software interrupt requests pending)

DATAV = non-selected PIR (PPB) data valid
DPPB = -DATAV, means the PPB is invalid

PPCV = physical PC (PPC) valid
DPPC = -PPCV, means the PPC is invalid

Table 2-1 (continued)

NA bit cleared	Activating condition
0	DOPS.IDX + ID1.DPPB + ID1SVC.(ID1+IRDF)
1	DOPS.SMO.IDX + ID1.(SOPS+DPPB) + ID1SVC.(ID1 + IRDF)
2	(DOPS.SMO.IDX + SOPS.ID1 + ID2).DMO + ID1.DPPB + ID1SVC.(ID1 + IRDF)
3	(JOPS + DPPB).ID1 + ID1SVC.(ID1 + IRDF)
4	DPPC.ID1 + ID1SVC.(ID1 + IRDF)
5	ID1SVC.(ID1 + IRDF)

The following QPLA AND terms are used in the Q logic:

NAF<9:0>, QIR<15:8>,QIR<7:0>

```
QPLA  0100111111,XXXXXXXX,XXXXXXXX    ;ID1
QPLA  0100111100,XXXXXXXX,XXXXXXXX    ;ID2
QPLA  0100111XXX,XXXXXXXX,XXXXXXXX    ;IDX
QPLA  0100110000,XXXXXXXX,XXXXXXXX    ;IRDF

QPLA  XXXXXXXXXX,XXXX000X,XXXXXXXX    ;SMO
QPLA  XXXXXXXXXX,XXXXXXXX,XX000XXX    ;DMO

QPLA  XXXXXXXXXX,00000000,11XXXXXX    ;SOP1:SWAB
QPLA  XXXXXXXXXX,X000101X,XXXXXXXX    ;SOP2:CLR(B) TO TST(B)
QPLA  XXXXXXXXXX,X0001100,XXXXXXXX    ;SOP3:ROR(B) TO ASL(B)
QPLA  XXXXXXXXXX,X0001101,X1XXXXXX    ;SOP4:MFPI,SXT,MFPD,MFPS
QPLA  XXXXXXXXXX,10001101,00XXXXXX    ;SOP5:MTPS
QPLA  XXXXXXXXXX,01110XXX,XXXXXXXX    ;SOP6:EIS:MUL,DIV,ASH,ASHC
QPLA  XXXXXXXXXX,0111100X,XXXXXXXX    ;SOP7:XOR
QPLA  XXXXXXXXXX,00001110,00XXXXXX    ;SOP8:CSM

QPLA  XXXXXXXXXX,X0X1XXXX,XXXXXXXX    ;DOP1:MOV(B),BIT(B)
QPLA  XXXXXXXXXX,XX10XXXX,XXXXXXXX    ;DOP2:CMP(B),ADD,SUB
QPLA  XXXXXXXXXX,X10XXXXX,XXXXXXXX    ;DOP3:BIC(B),BIS(B)

QPLA  XXXXXXXXXX,00000000,01XXXXXX    ;JOP1:JMP
QPLA  XXXXXXXXXX,0000100X,XXXXXXXX    ;JOP2:JSR

SOPS = SOP1+SOP2+SOP3+SOP4+SOP5+SOP6+SOP7+SOP8
DOPS = DOP1+DOP2+DOP3
JOPS = JOP1+JOP2
```

Table 2-1 (continued)

The Q logic in two level notation:

Term	Inputs																		Function	Outputs					
	IDI+IRDF	IDSVC	DPPC	DPPB	IID1	IID2	IIDX	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3		5	4	3	2	1	0
1	X	X	X	X	X	X	1	X	0	X	1	X	X	X	X	X	X	X	X	X	DOP1.IDX						0
2	X	X	X	X	X	X	1	X	X	1	0	X	X	X	X	X	X	X	X	X	DOP2.IDX						0
3	X	X	X	X	X	X	1	X	1	0	X	X	X	X	X	X	X	X	X	X	DOP3.IDX						0
4	X	X	X	X	X	X	1	X	0	X	1	0	0	0	X	X	X	X	X	X	DOP1.IDX.SMO					0	
5	X	X	X	X	X	X	1	X	X	1	0	0	0	0	X	X	X	X	X	X	DOP2.IDX.SMO					0	
6	X	X	X	X	X	X	1	X	1	0	X	0	0	0	X	X	X	X	X	X	DOP3.IDX.SMO					0	
7	X	X	X	X	X	X	1	X	0	X	1	0	0	0	X	X	X	0	0	0	DOP1.IDX.SMO.DMO				0		
8	X	X	X	X	X	X	1	X	X	1	0	0	0	0	X	X	X	0	0	0	DOP2.IDX.SMO.DMO				0		
9	X	X	X	X	X	X	1	X	1	0	X	0	0	0	X	X	X	0	0	0	DOP3.IDX.SMO.DMO				0		
10	X	X	X	X	1	X	X	0	0	0	0	0	0	0	0	1	1	X	X	X	SOP1.ID1					0	
11	X	X	X	X	1	X	X	X	0	0	0	1	0	1	X	X	X	X	X	X	SOP2.ID1					0	
12	X	X	X	X	1	X	X	X	0	0	0	1	1	0	0	X	X	X	X	X	SOP3.ID1					0	
13	X	X	X	X	1	X	X	X	0	0	0	1	1	0	1	X	1	X	X	X	SOP4.ID1					0	
14	X	X	X	X	1	X	X	1	0	0	0	1	1	0	1	0	0	X	X	X	SOP5.ID1					0	
15	X	X	X	X	1	X	X	0	1	1	1	0	X	X	X	X	X	X	X	X	SOP6.ID1					0	
16	X	X	X	X	1	X	X	0	1	1	1	1	0	0	X	X	X	X	X	X	SOP7.ID1					0	
17	X	X	X	X	1	X	X	0	0	0	0	1	1	1	0	0	0	X	X	X	SOP8.ID1					0	
18	X	X	X	X	1	X	X	0	0	0	0	0	0	0	0	1	1	0	0	0	SOP1.ID1.DMO				0		
19	X	X	X	X	1	X	X	X	0	0	0	1	0	1	X	X	X	0	0	0	SOP2.ID1.DMO				0		
20	X	X	X	X	1	X	X	X	0	0	0	1	1	0	0	X	X	0	0	0	SOP3.ID1.DMO				0		
21	X	X	X	X	1	X	X	X	0	0	0	1	1	0	1	X	1	0	0	0	SOP4.ID1.DMO				0		
22	X	X	X	X	1	X	X	1	0	0	0	1	1	0	1	0	0	0	0	0	SOP5.ID1.DMO				0		
23	X	X	X	X	1	X	X	0	1	1	1	0	X	X	X	X	X	0	0	0	SOP6.ID1.DMO				0		
24	X	X	X	X	1	X	X	0	1	1	1	1	0	0	X	X	X	0	0	0	SOP7.ID1.DMO				0		
25	X	X	X	X	1	X	X	0	0	0	0	1	1	1	0	0	0	0	0	0	SOP8.ID1.DMO				0		
26	X	X	X	X	1	X	X	0	0	0	0	0	0	0	0	0	1	X	X	X	JOP1.ID1			0			
27	X	X	X	X	1	X	X	0	0	0	0	1	0	0	X	X	X	X	X	X	JOP2.ID1			0			
28	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0	0	0	ID2.DMO				0		
29	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DPPC.ID1		0				
30	X	X	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DPPB.ID1			0	0	0	0
31	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ID1SVC.(ID1+IRDF)	0	0	0	0	0	0

A 0 under output column n denotes that NA bit <n> is discharged (zeroed).

2.3 Counter Logic

The counter is a sixteen-bit decrementer. It is parallel loaded from IMIB<12:5>, (together with eight high order zero bits) by an LCNTR microinstruction, or from IDAL<15:0> by an OUTS microinstruction with control bit<10> = 0. It is decremented by one in parallel with some operation in the Data chip by an operate microinstruction with control bit<11> = 0. If the counter will decrement to zero during a microcycle, NA bit<0> is discharged (zeroed) at the start of that microcycle. With this mechanism the microcode can perform both single- and multi-microinstruction loops. Note that the contents of the counter are modified only if the Control chip is selected.

2.4 Prefetch Logic

The prefetch logic consists of the PLA input registers and the predecode signal logic.

2.4.1 PLA Input Registers (PIR<16>, PIR[1:0]<15:0>)

The PLA derives its input from a two-part PLA input register (PIR). The high order bit of the PLA input register (PIR<16>) is defined by the following logic equation:

PIR<16> = (PWRFF + FPEFF +
acknowledged interrupts).-SSFF + CPFF.ID1

Its inputs are, in order, the power fail, and floating point exception flip-flops (see section 2.5.9), the output of the interrupt blocking logic (see section 2.5.5), the single-step flip-flop (see section 2.8.2), the coprocessor flip-flop (see section 2.8.1), and the ID1 signal (see section 2.2.3.3.5). Spurious interrupts will force PIR<16> if the single-step flip-flop is cleared.

The low order 16 bits of the PIR are actually a pair of sixteen-bit registers (PIR[1:0]<15:0>). At any instance, one of the two registers is selected for input to the PLA, while the other is deselected and is waiting for or contains the next instruction stream word.

PIR selection rules:

1. In the selected Control chip, at T150 of a microcycle which generated a NAF of 477, toggle the output select flip-flop. In the deselected Control chip(s), at T100 of a MPRDC-L microcycle, toggle the output select flip-flop.
2. From T125 to T-25 of any prefetch (RDI, RDF, operate . prefetch . DATAV=1), latch the input selected PIR from IDAL.
3. From T125 to T-25 of any OUTS microinstruction with bits<9>, <7>, <6>, or <5> = 0, latch the input deselected PIR from IDAL.
4. From T75 to T125 of all microcycles, update the input select latch with the opposite output select flip-flop information.
5. PIR<16> is gated at T-25 of every microcycle.

2.4.2 Predecode Signal Logic

At T0, the selected Control chip gates the ANDed result of ID1.DATAV.-ID1SVC onto output MPRDC-L. At T100, MPRDC-L is deasserted. During a chip select error (see Sec. 2.2.1.4) control chip 0 will drive MPRDC-L to a deasserted state.

2.5 Interrupt Service Logic

This logic performs recognition and priority arbitration on internal and external interrupts.

2.5.1 Processor Status Word (PS<7:4>)

A copy of the PS priority information <7:5> is maintained for use in interrupt control. A copy of the T-bit (PS<4>) is also maintained. The priority level field (bits<7:5>) controls masking of hardware and software interrupt requests by means of the interrupt blocking logic.

PS bits<7:4> are loaded directly from IDAL<7:4> during an OUTS microinstruction with control bit<11> = 0. The data is clocked into the PS at T-25. Thus the output of the interrupt blocking logic will not be valid until the end of the next microcycle.

PS bits<7:5> are also loaded from IDAL<7:5> when the PS is written into via its bus address (word or byte write to 17 777 776, identified by the explicit addressing logic (see section 2.5.3)), provided that the MABORT-L signal is not asserted. PS bit<4> is not affected during this operation. The data is clocked into the PS at T250.

2.5.2 Program Interrupt Requests (PIRQ<15:9>)

The Control chip keeps a copy of PIRQ<15:9> for use in interrupt control. PIRQ<15:9> are loaded from IDAL<15:9> when the PIRQ is written via its bus address (word write to 17 777 772 or byte write to 17 777 773, identified by the explicit addressing logic (see section 2.5.3)), provided that the MABORT-L signal is not asserted. The data is clocked into the PIRQ at T250.

2.5.3 Explicit Addressing Logic

This logic decodes the physical address on the IDAL during external write operations. At T50, MBS-H<1:0> and MDAL-H<15:0> are latched into BSFF<1:0> and the IDAL latch, respectively. Together with the current microinstruction, they are decoded to detect either a PS or PIRQ write reference. The PS explicit address is decoded as BSFF<1:0> = 11 and IDAL<12:0> = 17776. The PIRQ explicit address is decoded as BSFF<1:0> = 11 and IDAL<12:0> = 17772 for word cycles and BSFF<1:0> = 11 and IDAL<12:0> = 17773 for byte cycles. If either is detected, then the specified register is enabled to accept write data at T250.

2.5.4 Hardware Interrupt Request Flip-Flops (IRFF<3:0>, EVENTFF)

Five synchronizer flip-flops clock the hardware interrupt request inputs (MIRQ-H<3:0>, MEVENT-L) every microcycle at T50 and during stretched microcycles at Tx50 (and optionally at T150). Five hardware interrupt request flip-flops (IRFF<3:0>, EVENTFF) clock the output of the synchronizer flip-flops every microcycle at T100 and, during stretched microcycles, at Tx00. The outputs of IRFF<3:0> and EVENTFF are inputs to the interrupt blocking logic.

2.5.5 Interrupt Blocking Logic

This logic uses the PS priority information to selectively mask pending hardware interrupt requests (IRFF<3:0>) and program interrupt requests (PIRQ<15:9>). See Table 2-2.

Table 2-2

PS Masking of Interrupt Requests

PS<7:5>=	Hardware Interrupts Acknowledged	Program Interrupts Acknowledged
7	none	none
6	IRFF<3>	PIRQ<15>
5	IRFF<3:2>, EVENTFF	PIRQ<15:14>
4	IRFF<3:1>, "	PIRQ<15:13>
3	IRFF<3:0>, "	PIRQ<15:12>
2	IRFF<3:0>, "	PIRQ<15:11>
1	IRFF<3:0>, "	PIRQ<15:10>
0	IRFF<3:0>, "	PIRQ<15:9>

2.5.6 Parity Error Flip-Flop (PTYFF)

This flip-flop defines whether a parity error interrupt should occur. It is clocked every stretched microcycle at Tx00 and at T100 during an OUTC microinstruction with control bit<12> = 0:

- If the current microcycle is a demand bus cycle (see section 2.9.3), and if MPARITY-L is asserted and MABORT-L is not asserted, clock in a one. MPARITY-L is first clocked into a synchronizer flip-flop, PARITYFF, every 100ns at T50, T150, ..., T-50 and whose output is sampled at Tx00.

- If the current microcycle is an OUTC with control bit<12> = 0, clock in a zero.

- Otherwise, clock in the current value.

This flip-flop is an input into the gate which generates the ID1SVC signal into the Q logic.

2.5.7 Intermediate T-bit Flip-Flop (ITFF)

This flip-flop defines whether a T-bit trap should occur before the execution of the next macroinstruction. It is clocked every microcycle at T100:

- If the current microcycle is a predecode microcycle, or if the current microinstruction is an OUTC with control bit<9> = 0, clock in PS<4>.

- If the current microinstruction is an OUTC and control bit<11> = 0, clock in a zero.

- Otherwise, clock in the current value.

This flip-flop is an input into the gate which generates the ID1SVC signal into the Q logic.

2.5.8 Stack Overflow Flip-Flop (ISOVFF)

This flip-flop reflects whether a stack overflow has occurred. The flip-flop is clocked every microcycle at T125:

- If the current microinstruction is an I/O microcycle and MSOV/JA-L is asserted, clock in a 1.
- If the current microinstruction is OUTC and control bit<10> = 0, clock in a zero.
- Otherwise, clock in the current value.

This flip-flop is an input into the gate which generates the ID1SVC signal into the Q logic.

2.5.9 Power Fail, Halt, and Floating Point Exception Flip-Flops (PWRFF, HLTFF, FPEFF)

The MPWRF-L, MHALT-H, and MFPE-L signals are clocked by synchronizer flip-flops every 100ns at T50, T150, ..., T-50. The power fail (PWRFF), halt (HLTFF), and floating point exception (FPEFF) holding flip-flops latch the outputs of these flip-flops. These flip-flops are clocked every microcycle at T100 and during stretched microcycles at Tx00 and are inputs to the gate which generates the ID1SVC signal into the Q logic. PWRFF and FPEFF are also inputs to the gate which generates PIR<16>.

2.5.10 Loading Interrupt Service Information

In order for the microcode in the interrupt service routine to check which interrupt has occurred, all the interrupt service information is loaded into PIR<15:0> on an OUTS microinstruction with control bit<5> = 0. This is accomplished by loading the interrupt service information onto IDAL<15:0> at T125, and then strobing IDAL<15:0> into the selected PIR<15:0> at T-25. The correspondence between interrupt service information and PIR bits is shown in Table 2-3. Note that PIRQ bits <11:9>, after masking by the interrupt blocking logic, are OR'd together before being loaded into the PIR.

Table 2-3

Correspondence Between
Interrupt Service Information
and PIR<15:0>

PIR bit	Service Information
15	PTYFF output
14	PWRFF output
13	EVENTFF output
12	HLTFF output
11	FPEFF output
10	ITFF output
9	ISOVFF output
8	IRFF<3> as masked by blocking logic
7	IRFF<2> as masked by blocking logic
6	IRFF<1> as masked by blocking logic
5	IRFF<0> as masked by blocking logic
4	PIRQ<15> as masked by blocking logic
3	PIRQ<14> as masked by blocking logic
2	PIRQ<13> as masked by blocking logic
1	PIRQ<12> as masked by blocking logic
0	PIRQ<11> + PIRQ<10> + PIRQ<9> as masked by blocking logic

2.6 Abort Service Logic

This logic performs recognition and differentiation of aborts.

2.6.1 Abort Processing

Assertion of MABORT-L signifies an abort condition. Between T-25 and T200, the Data chip drives MABORT-L (MMU and address abort); at all other times (cache and main memory abort), external logic must synchronize MABORT-L with respect to the Data chip MCONT-L signal. When MABORT-L is asserted during a demand bus cycle (see section 2.9.3), the Control chip performs the following actions:

- Discharges (zeroes) NA bits<9:8,6,4:0> to force a transfer to an abort service routine (see section 2.2.3.1).
- Latches abort service information for analysis by the microcode (see below).
- Presets all ones (NOP microinstruction) into the IMI latch.
- Drives non-I/O microcycle code onto MAIO-H lines.

Thus the next microcycle is always a NOP, followed by the first microcycle of the abort service routine.

2.6.2 Abort Service Flip-Flops (ABFF<4:0>)

These flip-flops differentiate between the types of aborts. All of these flip-flops are cleared by MINIT-L and ABFF<4,2:0> are cleared during the beginning of any non-demand external I/O cycle (read, write, or prefetch). ABFF<3> is cleared during the beginning of any external I/O cycle. They are then clocked during demand bus cycles (see section 2.9.3) as shown in Table 2-4:

Table 2-4

Clocking of Abort Flip-Flops

Flip-flop	Name	Clocked at	Data
ABFF<4>	Early abort	T100	MABORT-L
ABFF<3>	Parity error	T250 to T-50	PARITYFF
ABFF<2>	Address error	T75	Word I/O cycle . MDAL<0>
ABFF<1>	I/O address	T75	BSFF<1> OR BSFF<0>
ABFF<0>	Late abort	T125, T-50	MABORT-L

where PARITYFF is the output of the MPARITY-L synchronizer flip-flop.

2.6.3 Loading Abort Service Information

In order for the microcode in the abort service routine to check which abort has occurred, all the abort service information (plus additional internal status) is loaded into PIR<15:0> on an OUTS microinstruction with control bit<6> = 0. This is accomplished by loading the abort service/status information onto IDAL<15:0> at T125, and then strobing IDAL<15:0> into the selected PIR<15:0> at T-25. The correspondence between abort service/status information and PIR bits is shown in Table 2-5.

Table 2-5

Correspondence Between
Abort Service/Status
Information and PIR<15:0>

PIR bit	Service/Status Information
15:13, 11:8, 6:5	all 0's or all 1's
12	HLTFF output
7	SSFF output
4	ABFF<4> - Early abort
3	ABFF<3> - Parity error
2	ABFF<2> - Address error
1	ABFF<1> - I/O address
0	ABFF<0> - Late abort

2.7 AIO Code Generation

The selected Control chip (or Control chip 0 during a chip select error) monitors the Microinstruction bus (IMI<21:0>) and generates address input/output (AIO) codes for the System Interface logic. These codes define what kind of cycle is occurring. There are four encoded control lines (MAIO-H<3:0>) (see Table 2-6). The MAIO-H lines are valid by T0 of a new microcycle and incorporate demand abort and DATAV information from the previous microcycle.

Table 2-6

AIO Codes

MAIO-H<3:0>	Definition/(Activation Condition)
1111	Non-I/O microcycle (none of the other conditions or during a demand abort)
1110	GP input (RDG microinstruction)
1101	Interrupt vector read (RDINTR microinstruction)
1100	I-stream read request [((Operate microinstruction and control bit<12> = 0) OR (RDI microinstruction)) AND (DATAV = 1)]
1011	Read-modify-write demand, no bus lock (RMW microinstruction and control bit<12> = 1)
1010	Read-modify-write demand, bus lock (RMW microinstruction and control bit<12> = 0)
1001	D-stream read demand (RD microinstruction)
1000	I-stream read demand (RDF microinstruction or (RDI microinstruction and DATAV = 0))
011x	GP byte write (Byte operate or byte literal microinstruction immediately following an AWG microinstruction)
010x	GP word write (Word operate or word literal microinstruction immediately following an AWG microinstruction)
001x	External byte write (Byte operate or byte literal microinstruction immediately following an AW, AWI, AWD, or RMW microinstruction that did not abort)
000x	External word write (Word operate or word literal microinstruction immediately following an AW, AWI, AWD, or RMW microinstruction that did not abort)

2.8 Coprocessor Support Logic

This section describes the special logic required to support a coprocessor such as a floating point accelerator.

2.8.1 Coprocessor Flip-Flop (CPFF)

This flip-flop is clocked every microcycle at T100 as follows:

- If the current microcycle is an OUTC with control bit<7> = 0, clock in control bit <5>.
- Otherwise, clock in the current value.

This flip-flop is an input into the gate which generates PIR<16>. This flip-flop is used by the microcode during instruction decode to determine whether a coprocessor (particularly a floating point accelerator) is present.

2.8.2 Single-Step Flip-Flop (SSFF)

This flip-flop is clocked every microcycle at T100 as follows:

- If the current microcycle is an OUTC with control bit<6>= 0, clock in control bit<5>.
- If the current microcycle is a predecode microcycle (MPRDC-L asserted), clock in a zero.
- Otherwise, clock in the current value.

This flip-flop is an input into the gates which generate ID1SVC and PIR<16>. It is used by the microcode to suppress interrupt recognition for one macroinstruction.

2.8.3 Floating Point Status Flip-flops (FPS<7:5>)

These flip-flops maintain a copy of the floating point single/double, short/long integer, round/truncate bits in the FPS Register (FPS<7:5>). These flip-flops are updated from MDAL<7:5> by an OUTS microinstruction with bit<12> = 0.

On a prefetch (provided the FPS mask programmable option is enabled) and on an OUTS microinstruction with bit<7> = 0, FPS<7:5> and CPFF are driven onto IDAL<15:12> and loaded into PIR<15:12>. In both cases, PIR<11:0> is loaded from MDAL<11:0>.

2.9 State Sequencer

The state sequencer keeps the Control chip synchronized with the other chips and the System Interface. Inputs to the state sequencer include MCLK, MBS-H<1:0>, MMAP-L, MSCTL-L, MDV-L, MMISS-L, MINIT-L, MABORT-L, and IMIB<21:5>.

2.9.1 Latched State

At T50 of any cycle, the Control chip latches MBS-H<1:0> into the bank select flip-flops (BSFF<1:0>).

2.9.2 Extended Microcycles

At T150, the state sequencer evaluates the following logic equation:

```
STALL = STIO + MMAP-L + MABORT-L.DEMAND +
        READ.(MMISS-L + MBS-H<1> + MBS-H<0> +
        BSFF<1> + BSFF<0>).(-MABORT-L)
```

where

STIO	=	current microinstruction is a stretched I/O microcycle (RDG, RDINTR, or write)
MMAP-L	=	I/O map enable signal (DMA grant)
MABORT-L	=	abort signal
DEMAND	=	current microinstruction is a demand bus operation (see section 2.9.3)
READ	=	current microinstruction is a read (AIO code = 1100 or 10xx, i.e., RD, RMW, RDF, RDI, or Operate microinstruction and control bit<12> = 0 and DATAV = 1)
MMISS-L	=	cache miss signal
MBS-H<1>	=	bank select signal (cache bypass)
MBS-H<0>	=	bank select signal (cache force miss)
BSFF<1:0>	=	bank select flip-flops

If the equation is true, the Control chip enters wait state. The current microcycle is extended beyond the normal four clock periods. Starting at T350, the Control chip samples MSCTL-L. If asserted, the Control chip waits two clock periods and then resamples. If not asserted, the Control chip exits wait state and resumes normal operations at T-25.

2.9.3 Demand Bus Cycles

A demand bus cycle includes bus writes (operate or literal microinstruction after an AW, AWI, AWD, or RMW microinstruction), data stream reads (RD or RMW microinstruction), demand instruction stream reads (RDF or (RDI and DATAV=0) microinstruction), and interrupt vector reads (RDINTR microinstruction).

2.10 Chip Initialization

Assertion of signal MINIT-L does the following:

- selects Control chip output drivers;
- causes Control chips to generate a jump to Control chip 0, address 0;
- deselects all Control chips;
- clears the abort service flip-flops (ABFF<4:0>);
- initializes the state sequencer to wait state.

As in other extended cycles, deassertion of MSCTL-L causes the Control chip to exit wait state and to resume normal operations at T-25.

2.11 Test Features

Assertion of the test inputs (TEST1-L, TEST2-L) places the Control chip in test mode.

TEST1-L	TEST2-L	MODE
H	H	normal mode
H	L	normal mode, outputs disabled
L	H	test mode, operate
L	L	test mode, load vector

If both test inputs are asserted, the Control chip reads in a 16-bit test vector from MDAL-H<15:0> and a 22-bit microinstruction from MIB-H<21:0>. The test vector is latched in the test register for further decoding and is interpreted as follows:

bit<15> Control vector select
0 = vector 0
1 = vector 1

Vector 0:

bits<14:12> NA<9:0> source
0 = NAF<9:0>
1 = Q logic, abort logic, enable RFS
2 = unused
3 = IMIB<14:5>
4 = unused
5 = unused
6 = IDAL<9:0>
7 = IDAL<15:10>, DATAV, PPCV, ID1SVC, PIR<16>

bit<11> NAF latch control
0 = normal operation
1 = load and latch NAF from bits<9:0> if bits<14:12> are not equal to 001

bit<10> IMI<21:0> source
0 = microstore output
1 = NAT<9:0>, QIRCLK0, QIRCLK1, PIRCLK0, PIRCLK1, 00000000 (enable MIB outputs)

bits<9:0> Source for NAF<9:0> when bit<11> = 1

Vector 1:

bit<14>	Parallel count 0 = normal counter operation 1 = <15:8> and <7:0> of Counter count in parallel
bit<13>	PLA AND disable and ROM decoder enable 0 = normal operation 1 = disable PLA AND enable and enable ROM decoder
bit<12>	Latch load control (load from bit<9:7>) 0 = load NA<9:7> latch 1 = load ROM latch<7:0>
bit<11>	NA<9:7> latch for select decoders 0 = normal operation 1 = latch bits<9:7> at select decoders
bit<10>	NA<7:0> latch at ROM decoder 0 = normal operation 1 = latch bits<7:0> at ROM decoder and enable ROM decoder
bit<9:0>	Bits used for loading the NA latches

The microinstruction is latched in the IMIB latch.

If only TEST1-L is asserted, the Control chip executes its normal microcycle using the data flow specified by the test register. This permits the routing of internal information to the MIB outputs for verification.

If neither test input is asserted, the Control chip executes its normal microcycle. The test register is ignored.

3.0 INTERFACE

3.1 Inputs

3.1.1 Clock (MCLK)

A 20 Mhz, MOS-level clock is used to control the chip's functions. A normal microcycle is composed of four clock periods (200 nanoseconds). During extended microcycles, the normal microcycle is stretched in two-clock period (100 nsec) increments until the Data chip deasserts MSCTL-L.

3.1.2 Micro Data and Address Lines (MDAL-H<15:0>)

All the Control chips receive addresses and data from MDAL-H<15:0>. The MDAL inputs connect to the Internal Data and Address Lines (IDAL<15:0>) through the IDAL latch.

3.1.3 Microinstruction Bus (MIB-H<21:0>)

The MIB-H<21:0> inputs receive microinstructions from the selected Control chip or from Control chip 0 during a chip select error. The MIB inputs connect to the Internal Microinstruction bus (IMIB<21:5>) via the Microinstruction bus (IMI<21:0>) and the IMIB latch.

3.1.4 Chip Select (MCSEL-L)

This input is precharged high by all Control chips and is sustained by Control chip 0. The currently selected Control chip drives MCSEL-L low following precharge. If MCSEL-L has not been driven low by mid microcycle, a select error has occurred. This condition forces Control chip 0 to generate a jump microinstruction to Control chip 0, address 1.

3.1.5 Stack Overflow/Jump Allow (MSOV/JA-L)

MSOV/JA-L provides information on whether the microinstruction currently executing in the Data chip took a conditional jump or whether a stack overflow occurred.

If the current microinstruction is a conditional jump, then the input is interpreted as Jump Allow. If the current microcycle is an I/O microcycle, then the input is interpreted as Stack Overflow. If neither case is true, then the input is ignored.

3.1.6 Initialize (MINIT-L)

This input is used by power up logic in order to synchronize the chip set and to force the Control chips to a known location in the control store. Assertion of MINIT-L causes Control chip 0 to generate a jump to chip 0, address 0. All Control chips are deselected, including Control chip 0; however Control chip 0 will drive the MIB-H, MAIO-H, and MPRDC-L outputs. The Control chip then enters wait state and samples for the deassertion of MSCTL-L. Deassertion of MSCTL-L signals that the next chip state is T-25.

3.1.7 Abort (MABORT-L)

This signal reports that an abort occurred during a memory operation. Both memory management errors (access violations, length errors, etc.) and bus errors (parity, NXM, etc.) for demand and request cycles are reported by this line. The Control chip must examine this signal in conjunction with the current microinstruction in order to determine what action should take place. On a demand cycle (see section 2.9.3), assertion of this signal clears bits <9:8,6,4:0> of the next address, forcing the microcode to one of four locations; and presets the IMI latch to all ones (NOP microinstruction). On a request cycle, it is an input to the DATAV logic. MABORT-L must be synchronized with respect to the assertion of Data chip signal MCONT-L.

3.1.8 Bank Select (MBS-H<1:0>)

These two signals are time multiplexed. At T50 of read and write cycles, they define the type of address information present on MDAL-H<15:0>:

00 = system memory address
01 = system board register address
10 = I/O device register address
11 = internal Data chip register address

At T150 of read and write cycles, they convey cache status:

MBS-H<1> = cache bypass
MBS-H<0> = force cache miss

3.1.9 Kill Prefetch Buffer (MKPB-L)

Assertion of this input clears the DATAV and PPCV flip-flops. The Data chip asserts MKPB-L when it detects a condition that invalidates the prefetch buffer. Note that PPCV is not cleared if the currently executing microinstruction is AOBC or SOBC.

3.1.10 Cache Miss (MMISS-L)

Assertion of MMISS-L indicates that the current cache access resulted in a cache miss. The Control chip only examines MMISS-L at T150 during external read microcycles.

3.1.11 Data Valid (MDV-L)

After T200 during stretched non-writes, this signal controls the IDAL latch. If MDV-L is high, the latch is open; if MDV-L is low, the latch is closed. The System Interface asserts MDV-L during extended read cycles to indicate that valid data is present on the MDAL.

3.1.12 Stretch Control (MSCTL-L)

During normal microcycles, MSCTL-L is asserted by the Data chip to indicate the existence of an extended microcycle, and deasserted to indicate the end of wait state. During initialization (MINIT-L asserted), MSCTL-L is asserted by the Data chip and then deasserted to synchronize the end of initialization.

3.1.13 I/O Map Enable (MMAP-L)

This signal is time multiplexed. If asserted at T50, it indicates that the I/O map is enabled (MMR3<5> = 1). If asserted at T150, it indicates that the current microcycle will stretch due to a DMA grant.

3.1.14 Predecode (MPRDC-L)

This signal is monitored by all Control chips for a predecode from the selected Control chip. It is asserted at T0 and deasserted at T100 during a predecode microcycle.

3.1.15 Interrupt Request<3:0> (MIRQ-H<3:0>)

These four signals read in the four levels of hardware interrupt requests. Interrupt level seven corresponds to MIRQ-H<3>, six to MIRQ-H<2>, five to MIRQ-H<1>, and four to MIRQ-H<0>. These signals are synchronized and latched internally.

3.1.16 Halt (MHALT-H)

This signal is a non-maskable service condition. It is interpreted by the microcode as an external halt. This signal is synchronized and latched internally.

3.1.17 Power Fail (MPWRF-L)

The signal is a non-maskable service condition. It is interpreted by the microcode as a power fail condition. This signal is synchronized and latched internally.

3.1.18 Floating Point Exception (MFPE-L)

This signal is a non-maskable service condition. It is interpreted by the microcode as a floating point coprocessor exception. This signal is synchronized and latched internally.

3.1.19 Bus Event (MEVENT-L)

This signal is a bus event interrupt request. It is interpreted by the microcode. This signal is synchronized and latched internally.

3.1.20 Parity Error (MPARITY-L)

This signal is tested during demand bus cycles (see section 2.9.3) to detect parity error interrupts and to differentiate a parity error abort from other aborts. If this signal is asserted without MABORT-L, a parity error interrupt is generated. If this signal is asserted simultaneously with MABORT-L, a parity error abort is generated.

3.1.21 Test Mode (TEST1-L, TEST2-L)

Assertion of TEST1-L causes the Control chip to enter test mode. Assertion of TEST2-L causes the Control chip to disable all outputs. If TEST1-L is also asserted, assertion of TEST2-L causes the Control chip to load in a test vector. These inputs are internally pulled to the high (inactive) state.

3.2 Outputs

3.2.1 Microinstruction Bus (MIB-H<21:0>)

This 22-bit bus is driven by the selected Control chip or by Control chip 0 at initialization and during a chip select error. It transmits the current microinstruction to all Control chips and to the Data chip.

3.2.2 Chip Select (MCSEL-L)

This signal is precharged high by all Control chips. Control chip 0 then sustains the high state with a small sustainer device. This signal is driven low by the selected Control chip to indicate that a Control chip is currently selected and is controlling the microprogram sequence. During initialization all control chips drive a high output on this signal.

3.2.3 Predecode (MPRDC-L)

This signal is driven by the selected Control chip or by Control chip 0 during a chip select error. During initialization all control chips drive a high output on this signal. It is driven at T0 with the ANDed result of ID1.DATAV.-ID1SYC. It is unconditionally deasserted at T100.

3.2.4 Address Input/Output Codes (MAIO-H<3:0>)

These outputs are driven by the selected Control chip or by Control chip 0 during a chip select error with information which identifies the current microcycle (see section 2.7). During initialization all control chips drive these signals high.

3.3 Signal Summary

Signal Name	Signal Type		Pin Numbers	Applicable DC Tests												
				VIH	VIL	VIHT	VILT	II	IILL	IISL	IOH	IOL	IOHT	IOS	IOZ	ICCSB
MCLK	MOS	I	tbs	y	y			y								
MDAL-H<15:0>	TTL	I				y	y	y								
MIB-H<21:0>	MOS	IO		y	y						y	y			y	
MCSEL-L	MOS	IO			y*					y*	y	y		y	y	
MSOV/JA-L	MOS	I		y	y			y								
MINIT-L	TTL	I				y	y	y								
MABORT-L	TTL	I				y	y	y								
MBS-H<1:0>	TTL	I				y	y	y								
MKPB-L	MOS	I		y	y			y								
MMISS-L	TTL	I				y	y	y								
MDV-L	TTL	I				y	y	y								
MSCTL-L	TTL	I				y	y	y								
MMAP-L	TTL	I				y	y	y								
MPRDC-L	TTL	IO				y	y				y	y	y		y	
MIRQ-H<3:0>	TTL	I				y	y	y								
MHALT-H	TTL	I				y	y	y								
MPWRF-L	TTL	I				y	y	y								
MFPE-L	TTL	I				y	y	y								
MEVENT-L	TTL	I				y	y	y								
MPARITY-L	TTL	I				y	y	y								
TEST1-L	MOS	I		y	y				y							
TEST2-L	MOS	I		y	y				y							
MAIO-H<3:0>	TTL	O										y	y		y	
power	na															y
ground	na			na												

*only for chip 0

4.0 DC Characteristics

Absolute Maximum Rating

Storage Temperature Range	-65 C to +150 C
Active Temperature Range	-55 C to +125 C
Supply Voltage	+7.0V
Input or Output Voltage Applied	V_{ss}-0.3V to V_{cc}+0.3V

Electrical Characteristics

Specified Temperature Range	0 C to +70 C
Specified Voltage Range	+4.75V to +5.25V
Test Conditions	Temperature = +70 C V_{ss} = 0V V_{cc} = +4.75V (except as noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IH}	High level MOS input	70% V_{cc}		V	
V_{IL}	Low level MOS input		30% V_{cc}	V	
V_{IHT}	High level TTL input	2.2		V	
V_{ILT}	Low level TTL input		0.6	V	
I_I	Input leakage current non-TEST inputs (note 1)	-10	10	uA	$0V \leq V_I \leq V_{cc}$
I_{ILL}	Input current TEST inputs (note 1)	.1	5	mA	V_I=0V
I_{OH}	Output current at high level	-2.0		mA	$V_0=V_{cc}-0.4$
I_{OL}	Output current at low level	2.0		mA	V_0=0.4V

I_{OHT}	Output current at high TTL level	-2.0		mA	V_O=2.4V
I_{ISL}	Sustainer current at low level		100	uA	V_I=30%V_{cc}
I_{OS}	High level sustainer current (note 1)	-0.2	-0.6	mA	$V_O=V_{cc}-1.0V$
I_{OZ}	Output leakage current (notes 1,2)	-10	10	uA	$0V \leq V_O \leq V_{cc}$
I_{CCSB}	Static power supply current (notes 1,3)		tbs	uA	
C_{IN}	Input capacitance (note 4)		5	pF	
C_{IO}	Input/output capacitance (note 4)		15	pF	
C_{OUT}	Output capacitance (note 4)		15	pF	

Note 1 - tested at V_{cc} = 5.25V.

Note 2 - only applies in the high impedance condition.

Note 3 - with TEST1-L, TEST2-L, and all outputs open circuit, all other inputs equal to V_{cc}.

Note 4 - sampled and guaranteed, but not tested. Does not apply to TEST1-L or TEST2-L.

5.0 AC Characteristics

Unless marked with an R (required), all AC characteristics are goals and are subject to further refinement.

Test Conditions

Temperature = +70 C
V_{ss} = 0V
V_{cc} = +4.75V (except as noted)
For output test loads, see Test Circuits

Timing Requirements

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{cyc}	clock cycle time (R)	50		ns	
t_{chi}	clock high width	18		ns	
t_{clo}	clock low width	18		ns	
t_{cr}	clock rise time		7	ns	
t_{cf}	clock fall time		7	ns	
t_{initw}	MINIT-L pulse width	tbs		ns	
t_{sctllh}	initialization interval	tbs		ns	
t_{sels}	MCSEL-L setup	25		ns	
t_{selh}	MCSEL-L hold	tbs		ns	
t_{mibs}	MIB-H setup	25		ns	
t_{mibh}	MIB-H hold	tbs		ns	
t_{ps}	MPRDC-L setup	25		ns	
t_{ph}	MPRDC-L hold	tbs		ns	
t_{ds}	MDAL-H<15:0> setup with respect to T50,T150,T225 (R)	20		ns	
t_{dh}	MDAL-H<15:0> hold with respect to T50,T225	20		ns	
t_{dhc}	MDAL-H<15:0> hold with respect to T150 (R)	5		ns	

t_{dvds}	MDAL-H<15:0> setup with respect to MDV-L	25		ns
t_{dvdh}	MDAL-H<15:0> hold with respect to MDV-L	25		ns
t_{hms}	MMISS-L setup (R)	20		ns
t_{hmh}	MMISS-L hold (R)	0		ns
t_{abse}	MABORT-L setup (early)	20		ns
t_{absl}	MABORT-L setup (late)	20		ns
t_{abh}	MABORT-L hold	0		ns
t_{jas}	MSOV/JA-L setup	20		ns
t_{jah}	MSOV/JA-L hold	0		ns
t_{bss}	MMAP-L,MBS-H<1:0> setup	20		ns
tb_{sh}	MMAP-L,MBS-H<1:0> hold	20		ns
t_{kps}	MKPB-L setup	20		ns
t_{kph}	MKPB-L hold	0		ns
t_{svcs}	MIRQ-H<3:0>,MHALT-H, MPWRF-L,MFPE-L, MEVENT-L setup (note 1)	20		ns
t_{svch}	MIRQ-H<3:0>,MHALT-H, MPWRF-L,MFPE-L, MEVENT-L hold (note 1)	20		ns
t_{scs}	MSCTL-L setup	20		ns
t_{sch}	MSCTL-L hold	20		ns
t_{pars}	MPARITY-L setup (note 1)	20		ns
t_{parh}	MPARITY-L hold (note 1)	20		ns
t_{dvpw}	MDV-L pulse width	25		ns
t_{dvf}	MDV-L fall time		15	ns

Timing Responses

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{prch}	MCSEL-L precharge		50	ns	test circuit 3
t_{seld}	MCSEL-L delay		50	ns	test circuit 3
t_{mibd}	MIB-H valid delay		50	ns	test circuit 3
t_{pd}	MPRDC-L valid delay (R)		50	ns	test circuit 2
t_{aiod}	MAIO-H<3:0> delay (R)		50	ns	test circuit 2
t_{dis}	transition to high impedance following chip deselect		25	ns	test circuit 1
t_{dist}	transition to high impedance following assertion of TEST2-L		tbs	ns	functional test
t_{ent}	transition from high impedance following deassertion of TEST2-L		tbs	ns	functional test

Note 1 - setup and hold requirements only to guarantee recognition at next sample point.

Appendix 1 - OUTS and OUTC Control Bits

The OUTS and OUTC microinstructions are used to control the internal logic of the Control chip. (For all other microinstruction definitions, see the Data Chip Specification.) Their control fields (bits<12:5>) are defined as follows:

OUTS - Output status

CF<5> = 0: load PIR from interrupt service information
1: no effect
(see Table 2-3)

CF<6> = 0: load PIR from abort service information
1: no effect
(see Table 2-5)

CF<7> = 0: load PIR from FPS<7:5>, CPFF, and MDAL<11:0>
1: no effect

CF<8> = 0: push MDAL<9:0> onto microsubroutine stack
1: no effect

CF<9> = 0: load PIR from MDAL<15:0>
1: no effect

CF<10> = 0: load counter from MDAL<15:0>
1: no effect

CF<11> = 0: load internal PS<7:4> from MDAL<7:4>
1: no effect

CF<12> = 0: load FPS<7:5> from MDAL<7:5>
1: no effect

OUTC - Output control

CF<5> = data value for CF<6> and CF<7>

CF<6> = 0: clock single-step flip-flop from CF<5>
1: no effect

CF<7> = 0: clock coprocessor flip-flop from CF<5>
1: no effect

CF<8> unused

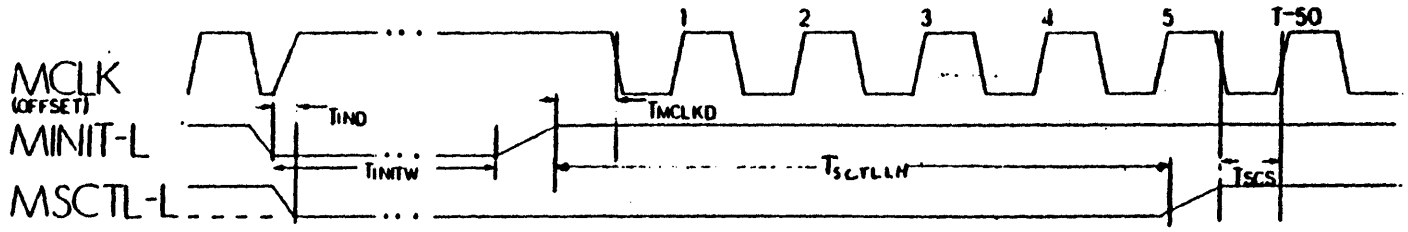
CF<9> = 0: load intermediate T-bit flip-flop from internal PS<4>
1: no effect

CF<10> = 0: clear stack overflow flip-flop
1: no effect

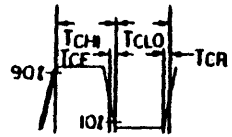
CF<11> = 0: clear intermediate T-bit flip-flop
1: no effect

CF<12> = 0: clear parity error flip-flop
1: no effect

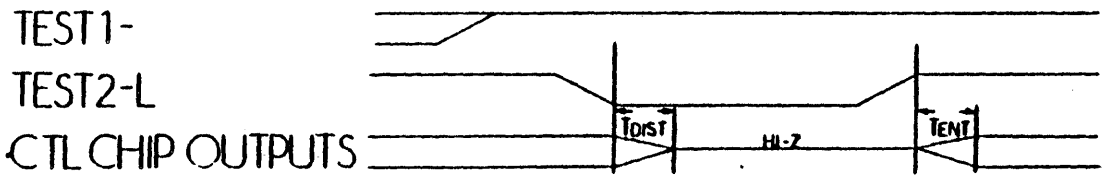
Note: Unused control bits may be either 1 or 0 during OUTS or OUTC microinstructions and must not have any effect on microinstruction operation either way.



INITIALIZATION SEQUENCE



CONTROL CHIP CLOCK INPUT WAVEFORM

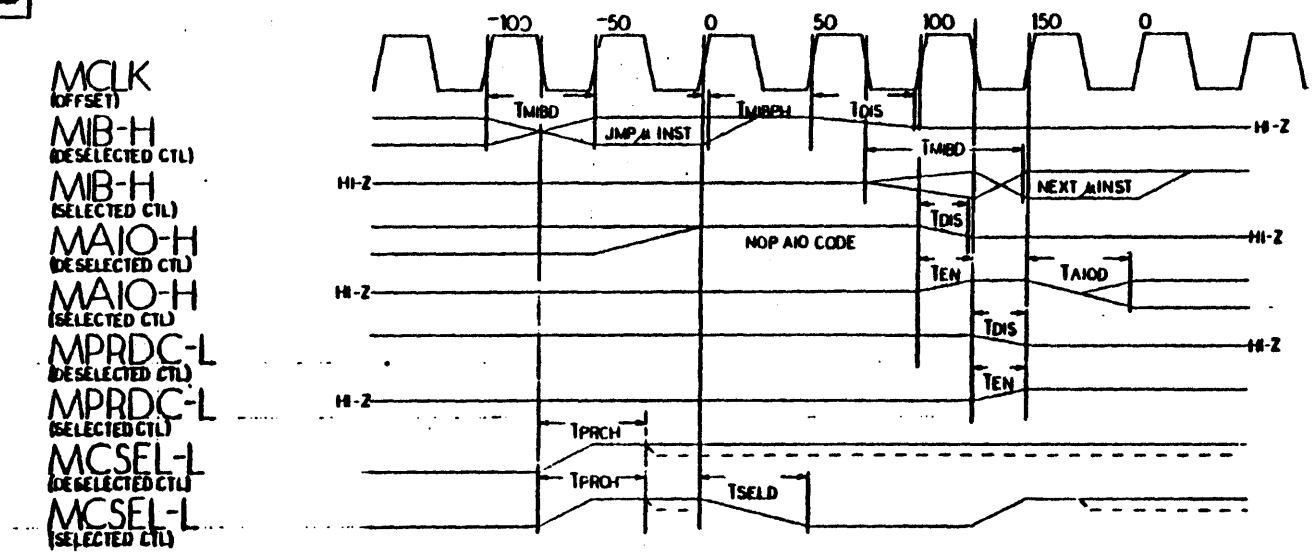


TEST TIMING

CONTROL CHIP TIMING WAVEFORMS 1

DEC-7-81

CONTROL CHIP TIMING



INTER CONTROL CHIP SIGNALS

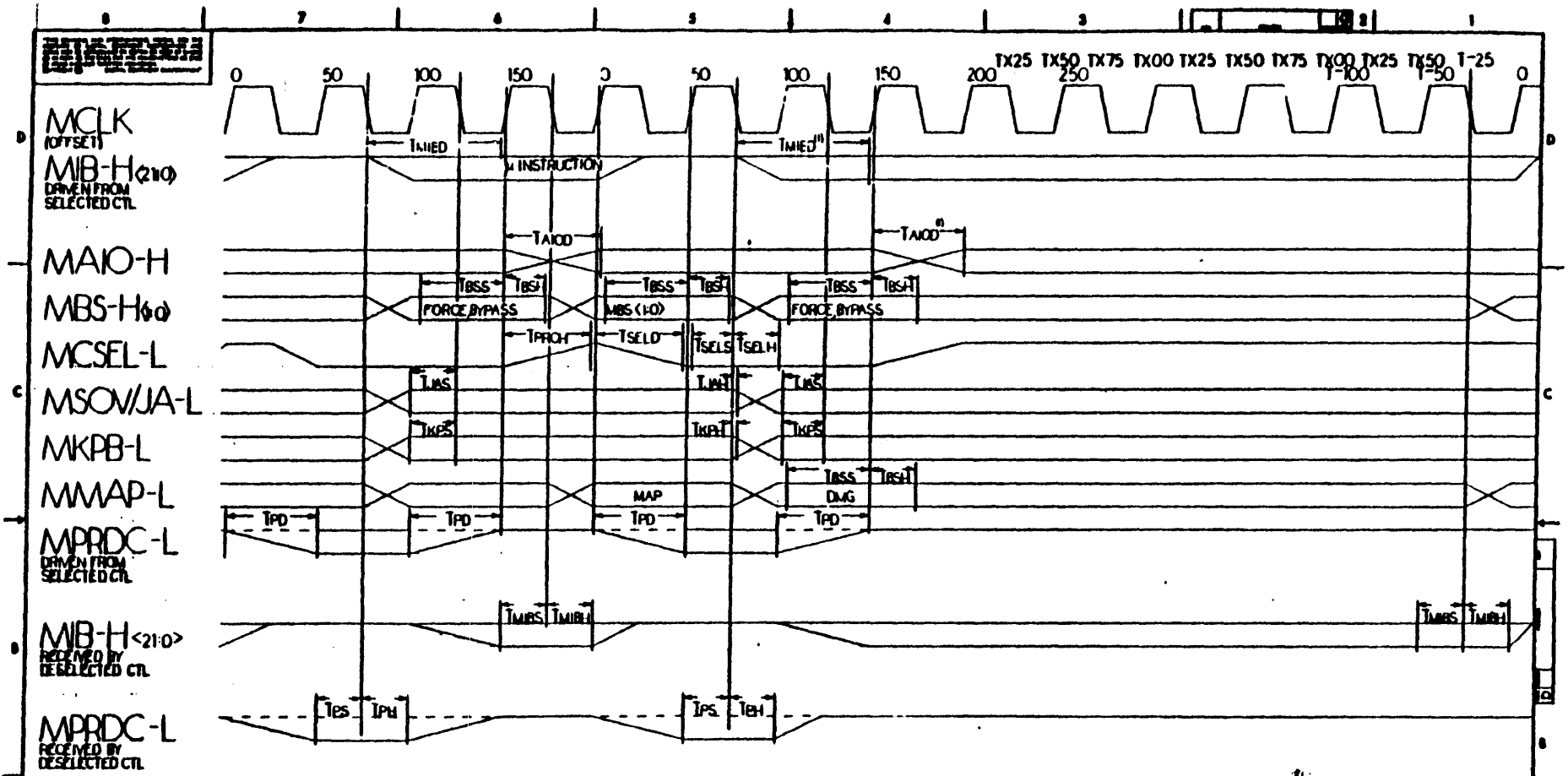
CONTROL CHIP TIMING WAVEFORMS 1B

11-28-32

CONTROL CHIP TIMING

D

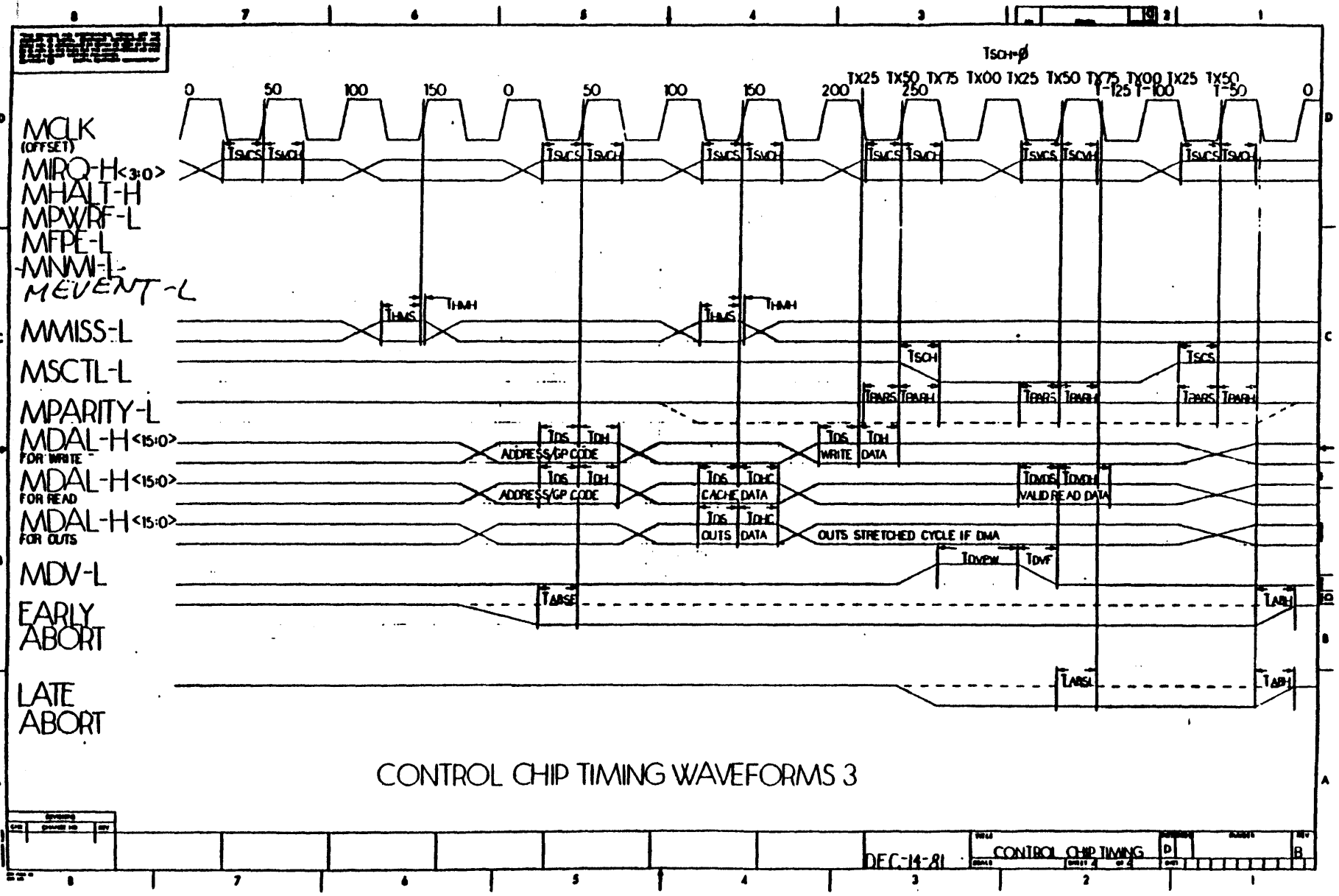
C



CONTROL CHIP TIMING WAVEFORMS 2

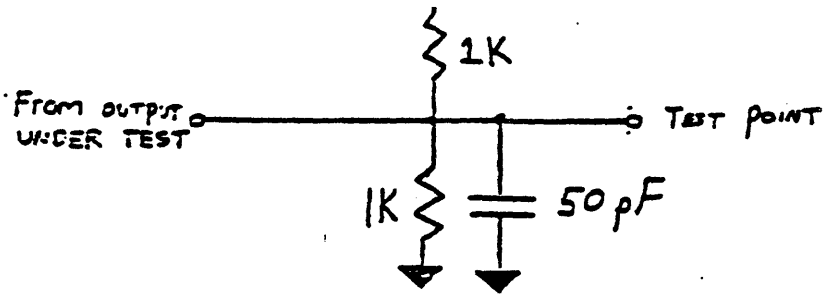
(1) MIB & AIO CODES CAN CHANGE AGAIN DURING STRECHED CYCLES IF A SYSTEM ABORT OCCURS

CONTROL CHIP TIMING

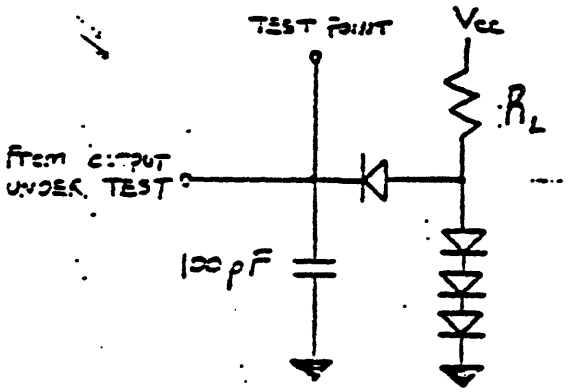


CONTROL CHIP TIMING WAVEFORMS 3

DEC-14-81 CONTROL CHIP TIMING



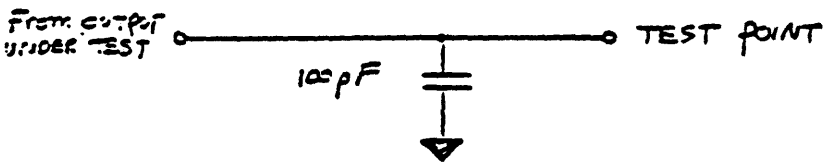
TEST CIRCUIT 1 - TRISTATE DISABLE.



ALL DIODES ARE EITHER 1N916 OR 1N3064.

R_L is selected to provide I_{OL} of 2 ma @ .4 volts.

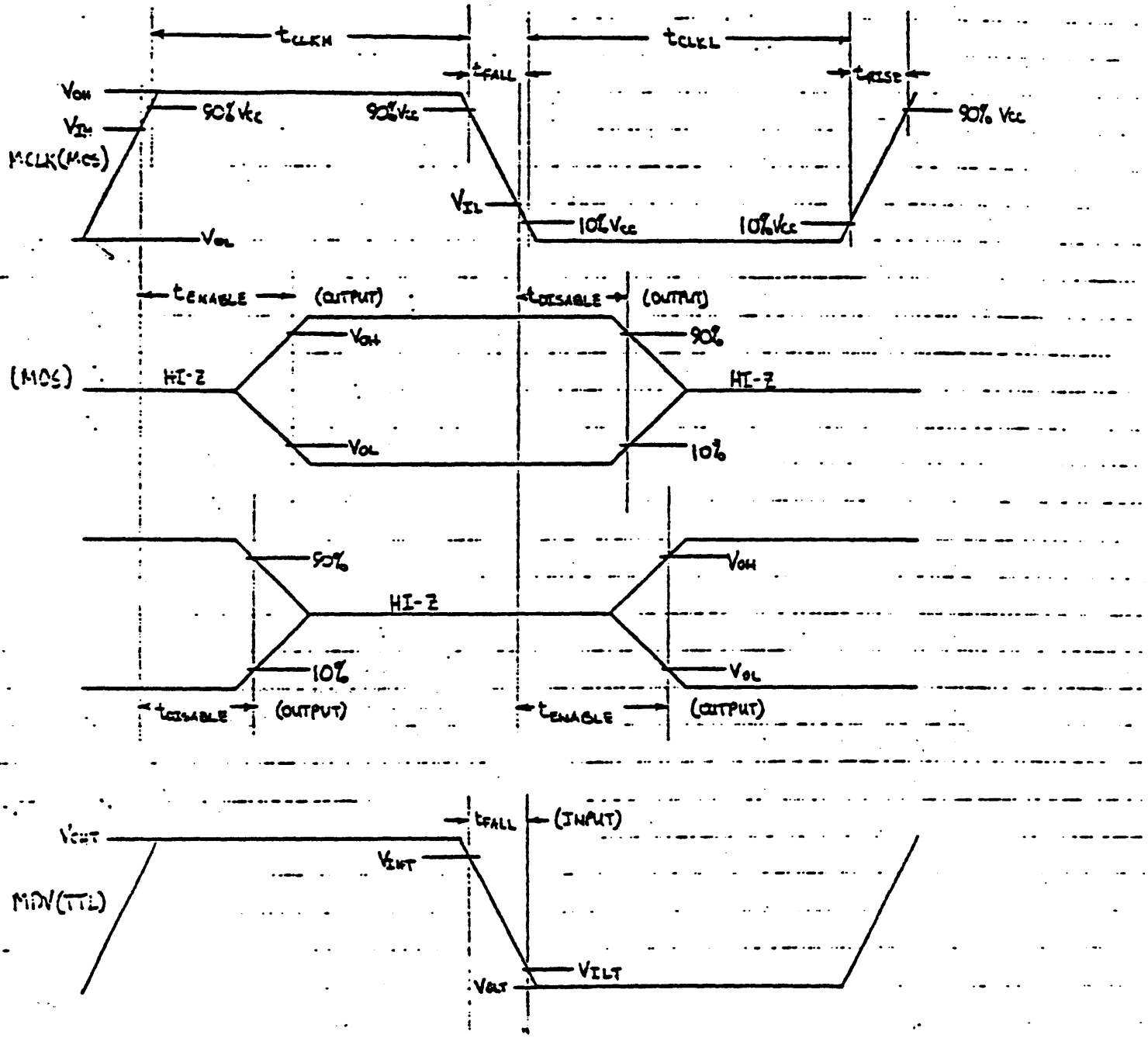
TEST CIRCUIT 2 - TTL OUTPUT



TEST CIRCUIT 3 - MOS OUTPUT

AC TEST CIRCUITS

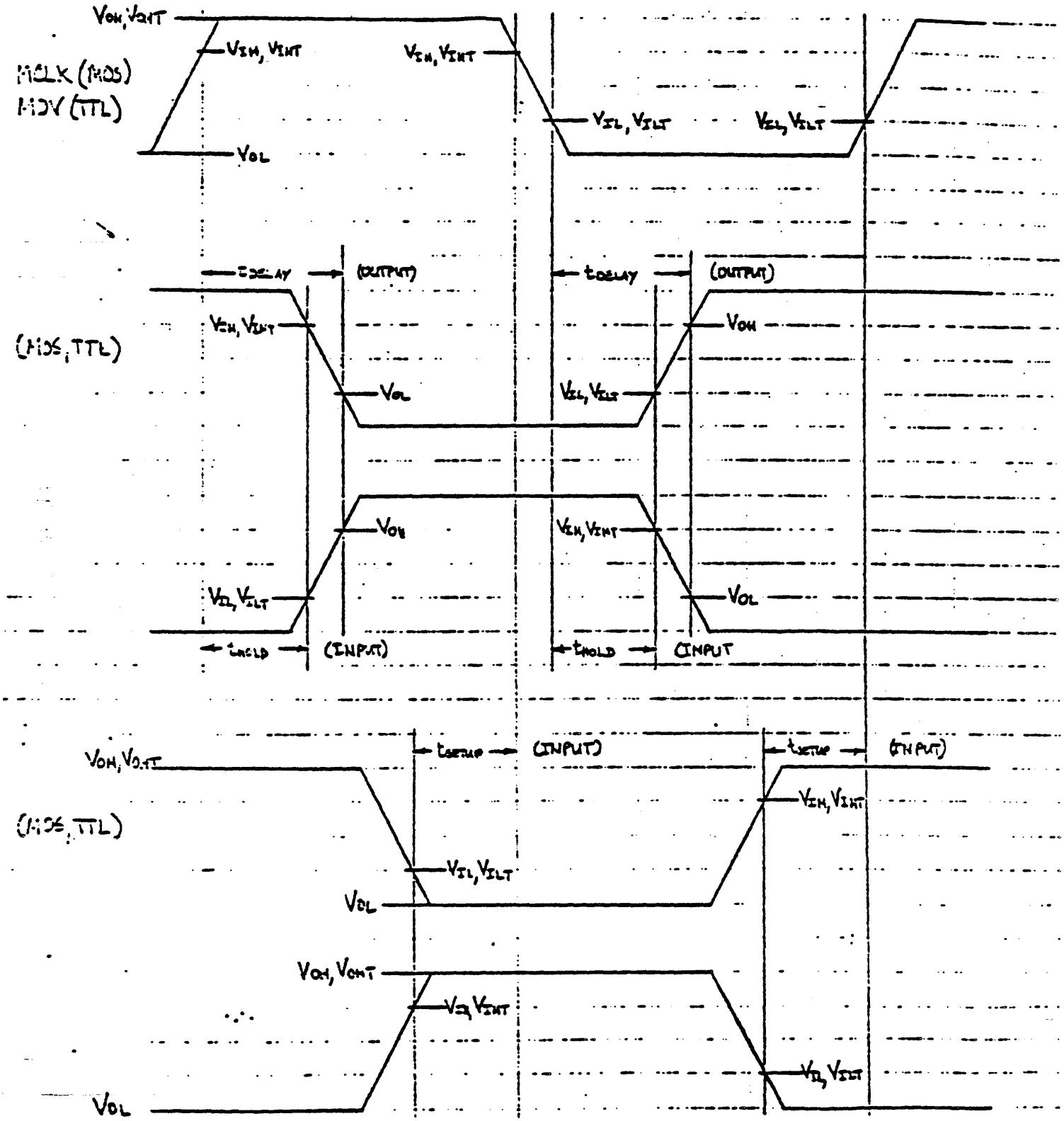
2/7/80



$V_{OH} = V_{CC} - 0.4v$

$V_{OL} = 0.4v$

1/24/81



$V_{OH} = V_{CC} - 0.4v$

$V_{OL} = 0.4v$

1/26/81